1 36598/PBH/B600 (BP 1096)

LARGE GAIN RANGE, HIGH LINEARITY, LOW NOISE MOS VGA

5 ABSTRACT OF THE DISCLOSURE

An integrated receiver with channel selection and image rejection is substantially implemented on a single CMOS integrated circuit. A receiver front end provides programable attenuation and a programable gain low noise amplifier. LC 10 filters integrated onto the substrate in conjunction with image reject mixers provide image frequency rejection. Filter tuning and inductor Q compensation over temperature are performed on chip. Active filters utilize multi track spiral inductors with shields to increase circuit Q. Frequency planning provides 15 additional image rejection. Local oscillator signal generation methods on chip reduce distortion. A PLL generates needed out of band LO signals. Direct synthesis generates in band LO signals. PLL VCOs are centered automatically. A differential crystal oscillator provides a frequency reference. Differential 20 signal transmission throughout the receiver is used. ESD protection is provided by a pad ring and ESD clamping structure. Shunts utilize a gate boosting at each pin to discharge ESD build up. An IF VGA utilizes distortion cancellation achieved with cross coupled differential pair amplifiers having their V_{ds} 25 dynamically modified in conjunction with current steering of the differential pairs sources.

LLW PAS231097.3-*-4/12/00 10:17 AM

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